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61 Experiment management support for performance tuning

Karen L. Karavanic, Barton P. Miller

November 1997 **Supercomputing '97:** Proceedings of the 1997 ACM/IEEE conference on Supercomputing (CDROM)

Publisher: ACM

Full text available: Pdf (69.59 KB) Additional Information: full citation, abstract, references, cited by

Bibliometrics: Downloads (6 Weeks): 4, Downloads (12 Months): 25, Downloads (Overall): 145, Citation Count: 4

The development of a high-performance parallel system or application is an evolutionary process. It may begin with models or simulations, followed by an initial implementation of the program. The code is then incrementally modified to tune its performance ...

62 Feedback-driven threading: power-efficient and high-performance execution of multi-threaded workloads on CMPs

M. Aater Suleman, Moinuddin K. Qureshi, Yale N. Patt

March 2008 **ASPLOS XIII:** Proceedings of the 13th international conference on Architectural support for programming languages and operating systems

Publisher: ACM Request Permissions

Full text available: Flv (22.0 MIN), Mp3 (9.55 MB), Pdf (275.90 KB) Additional Information: full citation, appendices and supplements, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 27, Downloads (12 Months): 194, Downloads (Overall): 693, Citation Count: 3

Extracting high-performance from the emerging Chip Multiprocessors (CMPs) requires that the application be divided into multiple threads. Each thread executes on a separate core thereby increasing concurrency and improving performance. As the number ...

Keywords: CMP, bandwidth, multi-threaded, synchronization

Also published in:

March 2008 **SIGOPS Operating Systems Review** Volume 42 Issue 2
March 2008 **SIGPLAN Notices** Volume 43 Issue 3
March 2008 **SIGARCH Computer Architecture News** Volume 36 Issue 1

63 Runtime monitoring on multicores via OASES

Vijay Nagarajan, Rajiv Gupta

April 2009 **SI GOPS Operating Systems Review** , Volume 43 Issue 2

Publisher: ACM

Full text available: Pdf (1.16 MB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 10, Downloads (12 Months): 117, Downloads (Overall): 117, Citation Count: 1

Runtime monitoring support serves as a foundation for the important tasks of providing security, performing debugging, and improving performance of applications. Often runtime monitoring requires the maintenance of information associated with each of ...

Keywords: atomic updates, exposed cache events, shadow memory

64 Performance of a multiband impulse radio UWB architecture

Martin Mittelbach, Rainer Moorfeld, Adolf Finger

October 2006 **Mobility '06:** Proceedings of the 3rd international conference on Mobile technology, applications & systems

Publisher: ACM

Full text available: Pdf (323.56 KB) Additional Information: full citation, abstract, references

Bibliometrics: Downloads (6 Weeks): 15, Downloads (12 Months): 58, Downloads (Overall): 146, Citation Count: 0

In this paper a highly flexible and scaleable multiband impulse radio UWB architecture for high data rates is described and evaluated. The investigations are mainly focused on on-off-keying modulation combined with a low-complexity non-coherent energy ...

Keywords: multiband impulse radio, non-coherent energy detection, on-off-keying, ultra-wideband

65 Interactive visibility culling in complex environments using occlusion-switches

Naga K. Govindaraju, Avneesh Sud, Sung-Eui Yoon, Dinesh Manocha

April 2003 **I3D '03:** Proceedings of the 2003 symposium on Interactive 3D graphics

Publisher: ACM Request Permissions

Full text available: Pdf (2.03 MB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 7, Downloads (12 Months): 39, Downloads (Overall): 492, Citation Count: 17

We present occlusion-switches for interactive visibility culling in complex 3D environments. An occlusion-switch consists of two GPUs (graphics processing units) and each GPU is used to either compute an occlusion representation or cull away primitives ...

Keywords: conservative occlusion culling, interactive display, levels-of-detail, multiple GPUs, parallel rendering

66 Integrating hardware and software concepts in a microprocessor-based system design lab

Steven K. Reinhardt

June 2000 **WCAE '00:** Proceedings of the 2000 workshop on Computer architecture education

Publisher: ACM

Full text available: Pdf (200.93 KB) Additional Information: full citation, abstract

Bibliometrics: Downloads (6 Weeks): 3, Downloads (12 Months): 22, Downloads (Overall): 71, Citation Count: 0

The EECS 373 "Design of Microprocessor-based Systems" course at the University of Michigan ties hardware and software together by providing a modern platform on which students simultaneously develop both hardware and software components of simple systems. ...

67 The WaveScalar architecture

Steven Swanson, Andrew Schwerin, Martha Mercaldi, Andrew Petersen, Andrew Putnam, Ken Michelson, Mark Oskin, Susan J. Eggers

May 2007 **Transactions on Computer Systems (TOCS)** , Volume 25 Issue 2

Publisher: ACM Request Permissions

Full text available: Pdf (898.53 KB) Additional Information: full citation, abstract, references, index terms

Bibliometrics: Downloads (6 Weeks): 21, Downloads (12 Months): 154, Downloads (Overall): 804, Citation Count: 2

Silicon technology will continue to provide an exponential increase in the availability of raw transistors. Effectively translating this resource into application performance, however, is an open challenge that conventional superscalar designs will not ...

Keywords: WaveScalar, dataflow computing, multithreading

68 Combined functional partitioning and communication speed selection for networked voltage-scalable processors

Jinfeng Liu, Pai H. Chou, Nader Bagherzadeh

October 2002 **ISSS '02:** Proceedings of the 15th international symposium on System Synthesis

Publisher: ACM

Full text available: Pdf (292.68 KB) Additional Information: full citation, abstract, references, index terms

Bibliometrics: Downloads (6 Weeks): 1, Downloads (12 Months): 8, Downloads (Overall): 324, Citation Count: 0

This paper presents a new technique for global energy optimization through coordinated functional partitioning and speed selection for embedded processors interconnected by a high-speed serial bus. Many such serial interfaces are capable of operating ...

Keywords: communication speed selection, communication/computation trade-offs, embedded multi-processor, functional partitioning, low-power design

69 Programming with(out) the GOTO

B. M. Leavenworth

November 1972 **SIGPLAN Notices** , Volume 7 Issue 11

Publisher: ACM

Full text available: Pdf (368.86 KB) Additional Information: full citation, abstract, references, cited by

Bibliometrics: Downloads (6 Weeks): 4, Downloads (12 Months): 29, Downloads (Overall): 314, Citation Count: 7

A brief history of the <u>goto</u> controversy (retention or deletion of the <u>goto</u> statement) is presented. After considering some of the theoretical and practical aspects of the problem, a summary of arguments both for ...

Keywords: <u>goto</u> statement, Markov algorithms, Post systems, Turuing machines, combinatory logic, computability theory, control structures, goto-less programming, lambda calculus, structured programming

70 Hardware/Software Co-testing of Embedded Memories in Complex SOCs

Bai Hong Fang, Qiang Xu, Nicola Nicolici

November 2003 **ICCAD '03:** Proceedings of the 2003 IEEE/ACM international conference on Computer-aided design

Publisher: IEEE Computer Society

Full text available: Pdf (145.29 KB) Additional Information: full citation, abstract, references, index terms

Bibliometrics: Downloads (6 Weeks): 0, Downloads (12 Months): 17, Downloads (Overall): 208, Citation Count: 0

A novel approach for testing embedded memories in complexsystems-on-a-chip (SOCs) is presented. The proposedsolution aims to balance the usage of the existing on-chipresources and dedicated design for test (DFT) hardwaresuch that the functional power ...

71 High-performance CUDA kernel execution on FPGAs

Alexandros Papakonstantinou, Karthik Gururaj, John A. Stratton, Deming Chen, Jason Cong, Wen-Mei W. Hwu

June 2009 **ICS '09: Proceedings of the 23rd international conference on Supercomputing**

Publisher: ACM Request Permissions

Full text available: Pdf (392.70 KB) Additional Information: full citation, abstract, references, index terms

Bibliometrics: Downloads (6 Weeks): 63, Downloads (12 Months): 226, Downloads (Overall): 226, Citation Count: 0

In this work, we propose a new FPGA design flow that combines the CUDA programming model from Nvidia with the state of the art high-level synthesis tool AutoPilot from AutoESL, to efficiently map the exposed parallelism in CUDA kernels onto reconfigurable ...

Keywords: coarse grained parallelism, cuda programming model, fpga, gpu, high level synthesis, high performance computing

72 On test data volume reduction for multiple scan chain designs

Sudhakar M. Reddy, Kohei Miyase, Seiji Kajihara, Irith Pomeranz

October 2003 **Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 8 Issue 4

Publisher: ACM Request Permissions

Full text available: Pdf (103.32 KB) Additional Information: full citation, abstract, references, index terms

Bibliometrics: Downloads (6 Weeks): 2, Downloads (12 Months): 31, Downloads (Overall): 354, Citation Count: 0

We consider issues related to the reduction of scan test data in designs with multiple scan chains. We propose a metric that can be used to evaluate the effectiveness of procedures for reducing the scan data volume. The metric compares the achieved compression ...

Keywords: Decompressor, Design for testability, Don't care identification, Encoding techniques, Test data compression

73 Programming with(out) the GOTO

B. M. Leavenworth

August 1972 **ACM '72: Proceedings of the ACM annual conference - Volume 2**, Volume 2

Publisher: ACM Request Permissions

Full text available: Pdf (380.83 KB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 4, Downloads (12 Months): 33, Downloads (Overall): 327, Citation Count: 15

A brief history of the goto controversy (retention or deletion of the goto statement) is presented. After considering some of the theoretical and practical aspects of the problem, a summary of arguments both ...

Keywords: Combinatory logic, Computability theory, Control structures, Goto statement, Goto-less programming, Lambda calculus, Markov algorithms, Post systems, Structured programming, Turing machines

74 POSC---a partitioning and optimizing SISAL compiler

Vivek Sarkar, David Cann

June 1990 **ICS '90: Proceedings of the 4th international conference on Supercomputing**

Publisher: ACM Request Permissions

Full text available: Pdf (1.42 MB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 16, Downloads (12 Months): 28, Downloads (Overall): 206, Citation Count: 6

Single-assignment languages like SISAL offer parallelism at all levels—among arbitrary operations, conditionals, loop iterations, and function calls. All control and data dependencies are local, and can be easily determined from the program. Various ...

Also published in:

September 1990 **SIGARCH Computer Architecture News** Volume 18 Issue 3b

75 Linear analysis and optimization of stream programs

Andrew A. Lamb, William Thies, Saman Amarasinghe

June 2003 **PLDI '03:** Proceedings of the ACM SIGPLAN 2003 conference on Programming language design and implementation

Publisher: ACM Request Permissions

Full text available: Pdf (489.80 KB) Additional Information: full citation, abstract, references, cited by, index terms

Bibliometrics: Downloads (6 Weeks): 7, Downloads (12 Months): 51, Downloads (Overall): 437, Citation Count: 7

As more complex DSP algorithms are realized in practice, there is an increasing need for high-level stream abstractions that can be compiled without sacrificing efficiency. Toward this end, we present a set of aggressive optimizations that target linear ...

Keywords: DSP, FFT, StreamIt, algebraic simplification, embedded, linear systems, optimization, stream programming

Also published in:

May 2003 **SIGPLAN Notices** Volume 38 Issue 5

76 Combined circuit architecture for computing normal basis and montgomery multiplications over GF (2^m)

Chin-Chin Chen, Chiou-Yng Lee, Erl-Huei Lu

September 2008 **Mobility '08:** Proceedings of the International Conference on Mobile Technology, Applications, and Systems

Publisher: ACM Request Permissions

Full text available: Pdf (400.65 KB) Additional Information: full citation, abstract, references, index terms

Bibliometrics: Downloads (6 Weeks): 3, Downloads (12 Months): 33, Downloads (Overall): 33, Citation Count: 0

Normal basis and Montgomery multiplications are two popular arithmetic operations in GF(2^m). In general, each element representation has its associated different algorithm and hardware multiplication architectures. In this paper, we will present ...

Keywords: bit-parallel systolic multiplier, hankel matrix-vector, montgomery, normal bases